Amendments to the Drawings:

The attached sheets of drawings include changes to Figs. 1-4. These sheets, which include Figs. 1-4, replaces the original sheets, including Figs. 1-4. In Figs. 1 and 2, a legend "(Background Art)" has been included to correct the drawings in compliance with the Office Action. In Fig. 3, the packets associated with the transaction "T4" have been included to correct the drawings in compliance with the Office Action. In Fig. 4, components 292, 290 and 296 and reference labels 228 have been incorporated to correct inconsistencies with the prepared specification (paragraph [030] on page 11 and paragraph [037] on page 13).

Attachments: 5 Replacement Sheets
4 Annotated Sheets Showing Changes

REMARKS

Claims 1-48 are pending. In the Office Action dated July 27, 2006, the Examiner took the following action: (1) objected to the drawings; (2) objected to claim 21 for informalities; (3) rejected claims 1-4, 6, 10-15, 17, 21-25, 28-32, 34 and 38-48 under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of U.S. Patent No. 5,748,629 to Caldara et al. ("Caldara"); and (4) rejected claims 5, 7-9, 16, 18-20, 26-27, 33 and 35-37 under 35 U.S.C. § 103(a) as being unpatentable over AAPA and Caldara, and in view of U.S. Patent No. 6,778,546 to Epps et al. ("Epps").

The disclosed embodiments of the invention will now be discussed in comparison to the prior art. Of course the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the prior art subject matter, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

The disclosed embodiment of the invention is directed to a memory hub architecture that includes a plurality of memory modules having a plurality of memory devices that are accessed through a memory hub to maximize the bandwidth of data buses. The memory hub controls access to the memory devices and efficiently routes memory requests and responses between the system controller and the memory devices through a high speed bus system. The disclosed memory hub architecture sends read or write data requests in a single packet that includes address, data, and control bits. The packetized memory request also includes a command header corresponding to a memory command for identifying the bits that specify the memory module to which the request is directed and the address of the memory devices in the specified memory module. The bandwidth of the bus system is better optimized by reorganizing groups of data to form the packets in a manner that substantially utilizes all the available capacity of the high speed bus, irrespective of the varying sizes of the groups of data that are received.

Figure 3 shows an embodiment of the invention for organizing and processing the packetized memory request data described above before the data is coupled to a downstream or an upstream high speed bus. A data organization unit 180 receives groups of data organized in 32-bit units, where each 32-bit data unit is known as a "lane." The total number of lanes in each

group varies, with each group representing a memory transaction T0-T4. For example, each of the transactions T0 and T1 contain 7 32-bit lanes, but transaction T2 contains 5 lanes and transaction T3 contains 12 lanes, and so on. The data organization unit 180 additionally assigns a command header CH to each group as each transaction T0-T4 is reorganized into packets. The packets are clocked out of the data organization unit 180 in parallel to maximize bandwidth, and then converted to serial data by a parallel-to-serial converter 182 onto a high speed bus. Instead of separating the packets according to the groups T0-T4, which would leave empty lanes in the parallel configuration due to the varying number of lanes in each transaction group, the data groups are packed together and organized by utilizing the full capacity of each parallel configuration by filling the vacant lanes in a lane group 190-198 with the next available lanes from the next group. For example, 6 lanes of the lane group 194 has been filled by the lanes of the transaction group T2, but since the transaction group T2 does not need all 8 lanes, the vacant two lanes remaining are filled by the next transaction group T3. The transaction group T3 then utilizes the next lane group 196 to fill with its remaining lanes. In the same manner, all the lanes in the lane groups 190-198 are filled to capacity as the data organization unit 180 forms the packets, and where the packets in the parallel configuration are separated by the command header CH instead of according to a lane group.

In contrast, the admitted prior art, referred to by the Examiner as "AAPA," describes a system for queuing groups of data as they are received and transferring the groups of data in the order they are received without any reorganization to the data. Consequently, the AAPA system leaves vacant lanes in the lane groups of the parallel configuration due to the varying number of lanes in the transactions T0-T4. The vacant lanes can cause idle periods of delay as the packets of data that are in parallel are converted to serial data and clocked onto the high speed bus. Therefore, due to the vacant slots in the lane groups of the parallel configuration while transferring over to the high speed bus, the AAPA system does not utilize the full capacity of the bus.

The Examiner has cited the Caldara reference, which discloses an asynchronous transfer mode (ATM) network switch capable of adaptively accommodating differing network traffic types having varying delay and bandwidth requirements. As each data cell is received by the input port of the ATM switch, the cell header is checked both for errors and to determine

whether it is associated with a valid connection. If the cell header is valid, then a queue number associated with the particular connection is assigned to transfer the data cell to the matching output port that places the data cell on a particular bus (constant bit rate, variable bit rate, available bit rate, or unspecified bit rate) (Col. 5, lines 55-65). If the cell header is deemed invalid, the bandwidth slotted for the invalid data cell may be replaced by a valid data cell to optimize the bandwidth (Col. 7, line 18 to Col. 8, line 31). In contrast to disclosed memory module, the data groups of the Caldara reference are not packed together in parallel and in a continuous manner as they are received to optimize vacant slots on the bus. Additionally, the data groups of the disclosed memory module are not assessed, separated, categorized or invalidated and replaced, thereby changing the order the data groups were received. Instead, the Caldara reference describes a completely different method for optimizing the bandwidth of several buses for a telecommunications network system that includes a plurality of input ports containing a plurality of buffers that are organized into a plurality of input queues, and that categorizes each data cell as it is received to the queue associated with a matched bus connection (Col. 4, lines 31-37). Furthermore, when the data cells are transferred "as available bandwidth is dynamically reallocated" on a queue designated the dynamic bandwidth list, the data cell or group of cells are reallocated out of order and are processed when space becomes available as shown in Figure 5. At best, the Caldara reference is more similar to the AAPA system than the Applicant's disclosed memory module, because the data cells are received in queue and transferred to an output port in the same form as it was received, and the data within the data cells are not reorganized in any way.

The Caldara reference is further distinguishable from the Applicant's disclosed memory module and the AAPA system in that the purpose of the ATM switch is to manage traffic flow to a plurality of buses having a plurality of bandwidth and delay requirements. The purported combination of the AAPA system and the Caldara reference is therefore not compatible. Both the AAPA system and the disclosed embodiments of the invention describe a system that converts packets of data arranged in a parallel configuration to a serial stream of data on a single high speed data bus, and not to a plurality of different buses. Applicant understands that motivation to modify a reference does not need to be expressly articulated by the cited references, although if there is motivation to combine or modify a reference such motivation is

usually expressly found in the references. However the Examiner still must articulate a credible motivation to modify the cited references, either from the express or implied teachings of the cited references or from knowledge commonly known to those of ordinary skill in the art. A reason has not been articulated why one of ordinary skill in the art would modify an ATM switch system as in the Caldara reference to a conventional memory hub system for routing memory requests into packets and onto a single high speed bus.

In summary, the combination of the AAPA system and the Caldara reference do not teach optimizing the bandwidth of a high speed bus by reorganizing groups of data to form data packets in a manner that substantially utilizes all the available capacity of the high speed bus irrespective of the varying sizes of the groups of data that are received.

Turning now to the claims, the patentably distinct differences between the cited references and the claim language will be specifically pointed out. Claims 1 and 29 recite, in part, a memory hub having a transmit interface that includes a data organization system organizing the command header and data into lane groups having a plurality of lanes so that all the lanes in each lane group are filled with either bits assigned as a command header or data. The data organization system is operable to convert each of the lane groups into a serial stream of lanes for optimized transmission. Neither the cited reference or the AAPA teach or suggest an organization system that optimizes a high speed bus by filling a plurality of lane groups to capacity and converts the plurality of lane groups to a serial stream of lanes. Furthermore, there is no motivation or suggestion for combining the Caldara reference and the AAPA to achieve the disclosed embodiments of the invention. The Caldara reference is directed to categorizing data cells into a plurality of queues to transfer to matched buses having different bandwidth requirements, which contradicts the AAPA system that describes converting a parallel group of data into a serial data stream onto a single high speed bus.

Claim 12 is directed to a memory hub that includes at least one transmit interface having a data organization system operable to organize a command header and data into groups, each of which contain a predetermined number of sub-groups of a predetermined size. The groups of data are organized such that each sub-group containing data for a first transaction is immediately followed by a sub-group contain either additional data for the first transaction or the command header for a second transaction "so that each group is filled with sub-groups

containing either command header bits or data bits." The organization system is operable to output the groups of data as a stream of sub-groups of data. As previously described, the Caldara reference does not describe a data organization system that reorganizes sub-groups to fill the capacity of a group having a predetermined number of sub-groups of a particular size. In fact the data cells described in the Caldara reference are not queued in a continuous manner, but instead are categorized out of order and placed in different queues depending on the associated bus from a plurality of buses or depending on space availability. The AAPA system additionally does not describe organizing sub-groups of data for a first transaction followed by a second transaction to fill capacity of the group. Furthermore, there is no motivation or suggestion to combine the Caldara reference with the AAPA since they are not compatible, as previously explained.

Claim 23 is directed to a data organization system having a data organization unit that organizes a plurality of memory transactions into lane groups, each of which contain a plurality of lanes. The data is organized so that all the lanes in each lane group are filled with either command header bits or data bits. The AAPA system does not describe filling all the lanes in each lane group. In contrast to both the disclosed memory module and the AAPA system, the Caldara reference describes a categorization method for placing data cells in a plurality of queues that are organized according to a plurality of buses having different bandwidth requirements, as previously described. Furthermore, there is no motivation or suggestion to combine the Caldara reference with the AAPA for reasons stated above.

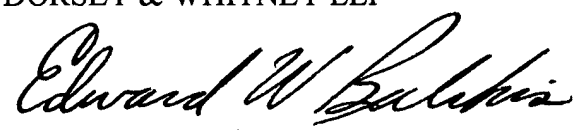
Claim 40 describes a method for organizing a command header and data into groups, each of which contain a predetermined number of sub-groups, and for transmitting the groups as a serial stream of sub-groups. The combination of the AAPA system and the Caldara reference do not teach organizing groups of data by sub-groups and transmitting the data as a serial stream of sub-groups, as previously described. In fact, the combination of the references is not compatible because the Caldara reference is directed to categorizing a plurality of data cells into a plurality of queues assigned to one of a plurality of buses having different bandwidth requirements. There is no motivation or suggestion to combine the Caldara reference with the AAPA for reasons previously stated.

Claims depending from claims 1, 12, 23, 29 and 40 are also allowable over the cited references due to depending from an allowable base claim and further in view of the additional limitations recited in the dependent claims.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



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EWB:dms

Enclosures:
Postcard
Fee Transmittal Sheet (+copy)
5 Replacement Sheets, Figs. 1-5
4 Annotated Sheets, Figs. 1-4

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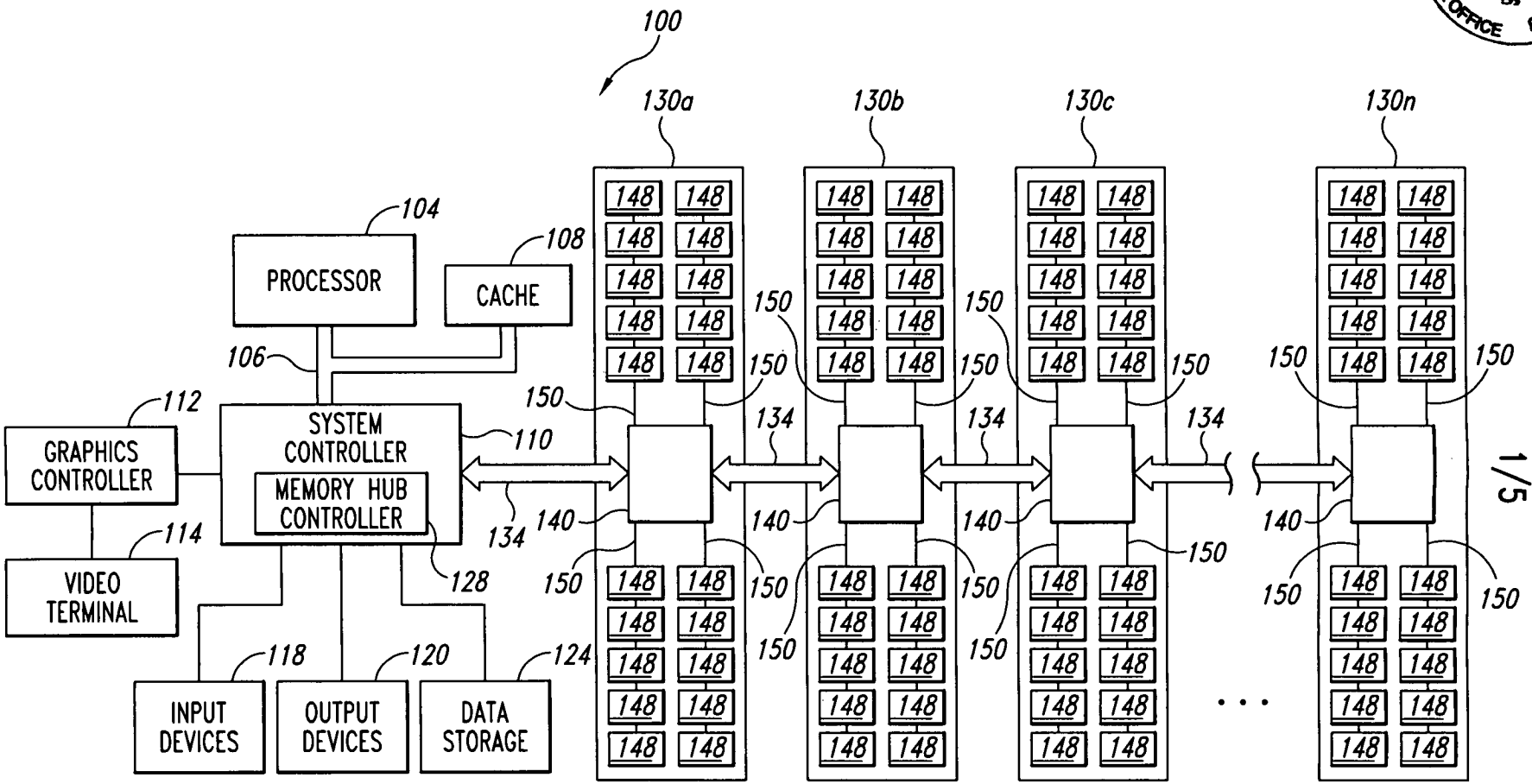


Fig. 1

(BACKGROUND ART)

1/5

Annotated Sheet Showing Changes

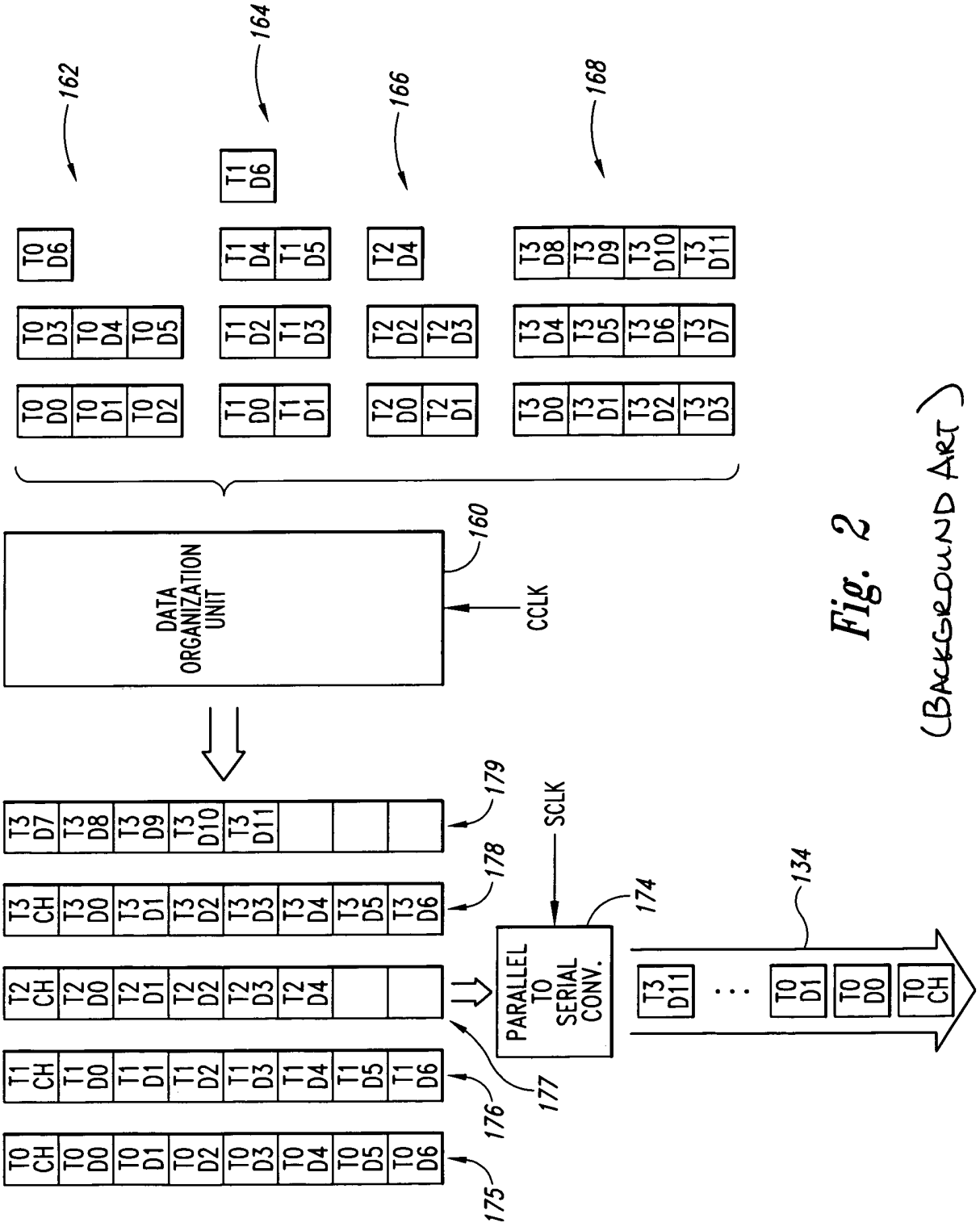
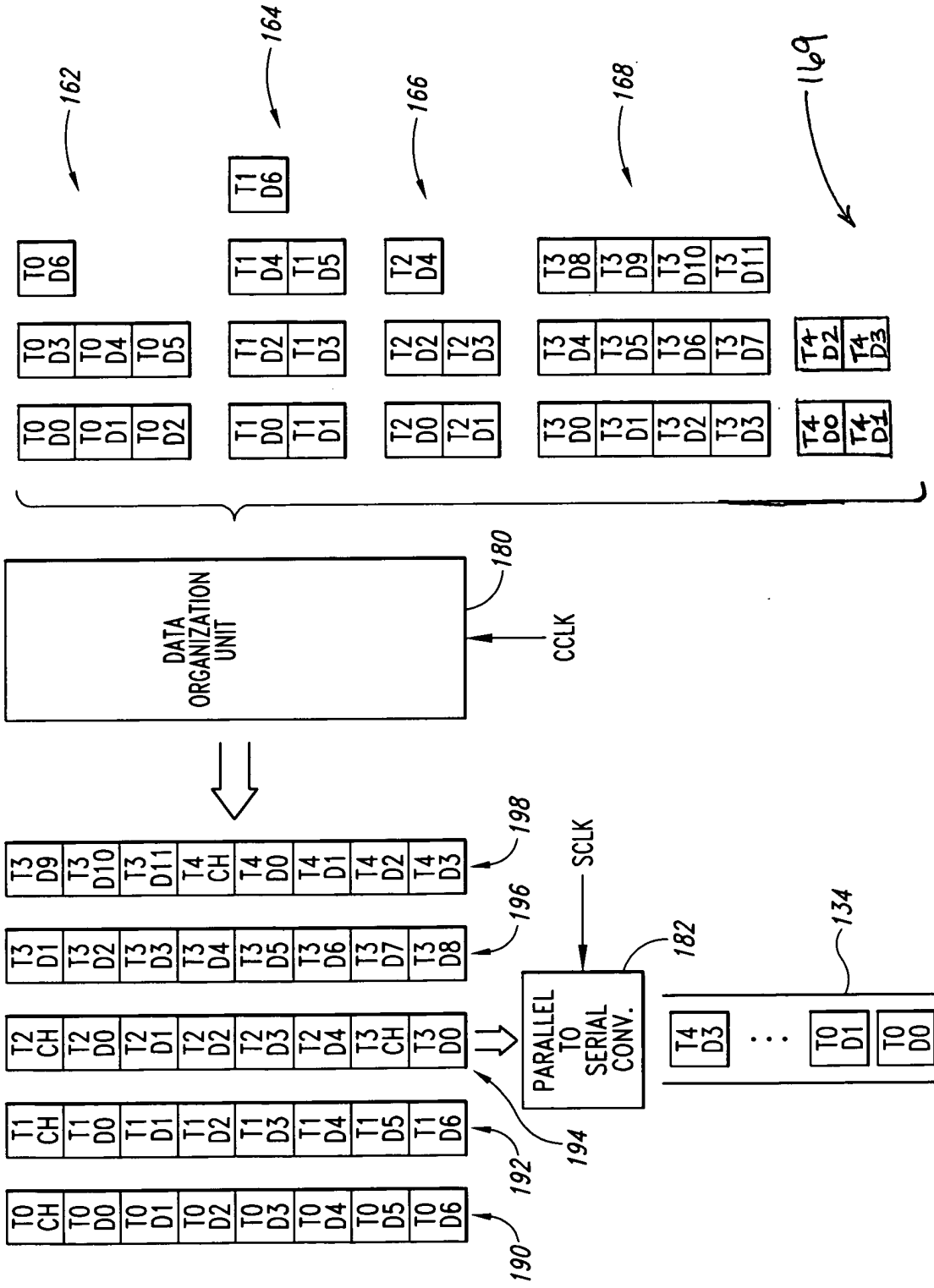


Fig. 2
(BACKGROUND ART)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164
166
168
169
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T0 D4
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T0 D0
T0 D1
T0 D2
T1 D6
T1 D4
T1 D5
T1 D2
T1 D3
T1 D0
T1 D1
T2 D4
T2 D2
T2 D3
T2 D0
T2 D1
T3 D8
T3 D9
T3 D10
T3 D11
T3 D4
T3 D5
T3 D6
T3 D7
T3 D0
T3 D1
T3 D2
T3 D3
T4 D2
T4 D3
T4 D0
T4 D1
DATA ORGANIZATION UNIT
180
CCLK
T3 D9
T3 D10
T3 D11
T4 CH
T4 D0
T4 D1
T4 D2
T4 D3
198
T3 D1
T3 D2
T3 D3
T3 D4
T3 D5
T3 D6
T3 D7
T3 D8
196
T2 CH
T2 D0
T2 D1
T2 D2
T2 D3
T2 D4
T3 CH
T3 D0
T1 CH
T1 D0
T1 D1
T1 D2
T1 D3
T1 D4
T1 D5
T1 D6
T0 CH
T0 D0
T0 D1
T0 D2
T0 D3
T0 D4
T0 D5
T0 D6
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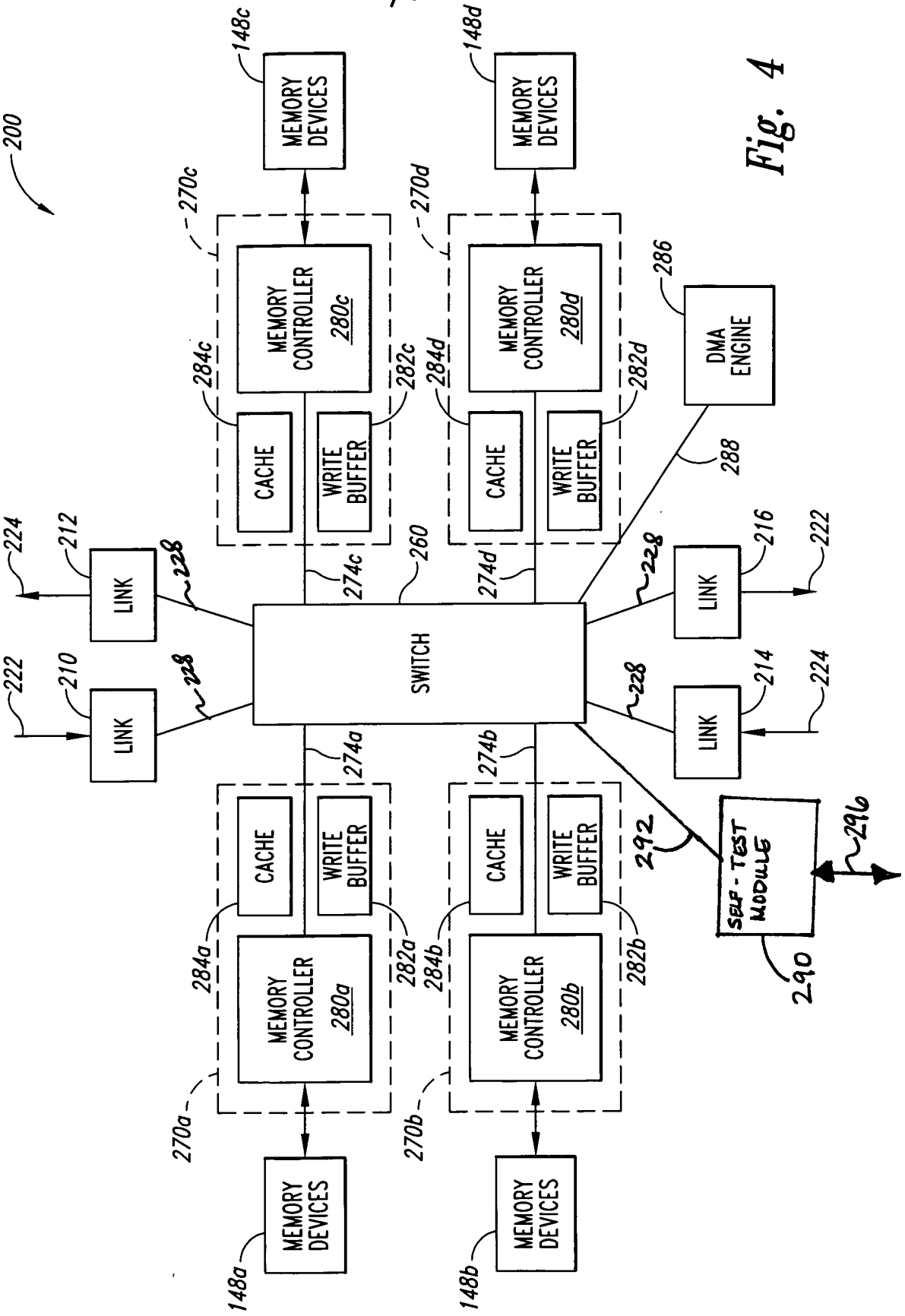
192
194
SCLK
PARALLEL TO SERIAL CONV.
182
134
T4 D3
T0 D1
T0 D0
T0 CH

Fig. 3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MEMORY DEVICES
148d
MEMORY DEVICES
270c
270d
MEMORY CONTROLLER 280c
MEMORY CONTROLLER 280d
284c
282c
284d
282d
CACHE
WRITE BUFFER
CACHE
WRITE BUFFER
286
DMA ENGINE
288
224
212
LINK
228
274c
260
274d
228
LINK
216
222
222
210
LINK
228
SWITCH
228
LINK
214
224
274a
274b
CACHE
WRITE BUFFER
CACHE
WRITE BUFFER
292
SELF-TEST MODULE
296
290
284a
282a
284b
282b
MEMORY CONTROLLER 280a
MEMORY CONTROLLER 280b
270a
270b
MEMORY DEVICES
148a
MEMORY DEVICES
148b

Fig. 4